Amendments to the Claims:

Please amend claims 1, 3, 4, and 7 as follows, and please add claims 10-24 as follows. This listing of claims replaces all prior versions, and listings, of claims in the application.

Listing of claims:

1. (currently amended) A method of fabricating a non-volatile semiconductor memory device comprising:

forming a charge storage layer on a substrate;

forming a control gate layer on the charge storage layer;

forming a gate mask in the shape of a spacer on the control gate layer; [[and]]

removing the charge storage layer and the control gate layer to expose a top portion of the substrate, wherein the gate mask protects a portion of the charge storage layer and the control gate layer to form a control gate and a charge storage region[[.]];

forming a conductive region in the top portion of the substrate;

forming a source-side insulative spacer on the top portion of the substrate adjacent a sidewall of the control gate and the charge storage region; and

forming a source electrode on the conductive region, wherein the source electrode is electrically isolated from the control gate and the charge storage region by the source-side insulative spacer, and wherein a top of the source electrode is at the same level as, or below, a top portion of the gate mask.

2. (original) The method of claim 1, wherein forming the gate mask comprises:

forming a disposable pattern on the control gate layer;

forming a gate mask layer on the disposable pattern and the control gate layer; and

removing a portion of the gate mask layer to form a gate mask on a sidewall of the disposable pattern.

3. (currently amended) The method of claim [[2]]1, wherein removing the charge storage layer and the control gate layer comprises:

etching the charge storage layer and the control gate layer using the gate mask and the disposable pattern as a etching mask thereby protecting a remaining portion of ~~remaining~~ the charge storage layer and the control gate layer under the gate mask and the disposable pattern;

removing the disposable pattern; and

etching the remaining portion of the charge storage layer and the control gate layer using the gate mask as an etching mask thereby forming a control gate and a charge storage region under the gate mask.

4. (currently amended) The method of claim [[3]]1 wherein the conductive region comprises a source, and wherein forming the source-side insulative spacer further comprises ~~comprising~~:

~~forming a source in the substrate adjacent to a sidewall of the control gate; and~~

forming a source-side spacer layer; and

forming [[a]] the source-side insulative spacer on the sidewall[[s]] of the control gate and the charge storage region by etching the source-side spacer layer.[[;]]

~~forming a source electrode on the source, wherein the source electrode is isolated from the control gate and the charge storage region by the source side spacer.~~

5. (original) The method of claim 1 further comprising forming a select gate on a sidewall of the charge storage region.

6. (original) The method of claim 5, wherein the select gate is in the shape of a spacer.

7. (currently amended) The method of claim 5 further comprising:

forming an LDD region in the substrate using the select gate as a LDD implantation mask; and

forming [[a]]an LDD spacer on a sidewall of the select gate.

8. (original) The method of claim 1, wherein forming the charge storage layer comprises:

forming a floating gate dielectric layer on the substrate;

forming a floating gate layer on the floating gate dielectric layer; and

forming an inter poly dielectric layer on the floating gate layer.

9. (original) The method of claim 1, wherein forming the charge storage layer comprises forming an ONO layer on the substrate.

10. (new) The method of claim 1, wherein forming the source electrode comprises:

forming a source electrode layer on the substrate; and

etching back the source electrode layer to form the source electrode.

11. (new) The method of claim 1, wherein forming the source electrode comprises:

forming a source electrode layer on the substrate; and

chemical mechanical polishing (CMP) the source electrode layer to form the source electrode.

12. (new) A method of fabricating a non-volatile semiconductor memory device comprising:

forming a charge storage layer on a substrate;

forming a control gate layer on the charge storage layer;

forming a gate mask in the shape of a spacer on the control gate layer;

removing the charge storage layer and the control gate layer to expose a top portion of the substrate, wherein the gate mask protects a portion of the charge storage layer and the control gate layer to form a control gate and a charge storage region;

forming a conductive region in the top portion of the substrate;

forming a source-side insulative spacer on the top portion of the substrate adjacent a first sidewall of the control gate and the charge storage region;

forming a source electrode on the conductive region, wherein the source electrode is electrically isolated from the control gate and the charge storage region by the source-side insulative spacer; and

forming a select gate on a second sidewall of the charge storage region.

13. (new) The method of claim 12, wherein a top of the source electrode is at the same level as, or below, a top portion of the gate mask.

14. (new) The method of claim 12, wherein forming the gate mask comprises:

forming a disposable pattern on the control gate layer;

forming a gate mask layer on the disposable pattern and the control gate layer; and

removing a portion of the gate mask layer to form a gate mask on a sidewall of the disposable pattern.

15. (new) The method of claim 12, wherein removing the charge storage layer and the control gate layer comprises:

etching the charge storage layer and the control gate layer using the gate mask and the disposable pattern as a etching mask thereby protecting a remaining portion of the charge storage layer and the control gate layer under the gate mask and the disposable pattern;

removing the disposable pattern; and

etching the remaining portion of the charge storage layer and the control gate layer using the gate mask as an etching mask thereby forming a control gate and a charge storage region under the gate mask.

16. (new) The method of claim 12 wherein the conductive region comprises a source, and wherein forming the source-side insulative spacer further comprises:

forming a source-side spacer layer; and

forming the source-side insulative spacer on the sidewall of the control gate and the charge storage region by etching the source-side spacer layer;

17. (new) The method of claim 12, wherein the select gate is in the shape of a spacer.

18. (new) The method of claim 17, wherein forming the select gate comprises:
forming a select gate layer on the substrate; and
anisotropically etching the select gate layer to form the select gate.

19. (new) The method of claim 18, wherein the select gate layer comprises a doped polycrystalline silicon material.

20. (new) The method of claim 12 further comprises:
forming an LDD region in the substrate using the select gate as a LDD implantation mask; and
forming an LDD spacer on a sidewall of the select gate.

21. (new) The method of claim 12, wherein forming the charge storage layer comprises:
forming a floating gate dielectric layer on the substrate;
forming a floating gate layer on the floating gate dielectric layer; and
forming an inter poly dielectric layer on the floating gate layer.

22. (new) The method of claim 12, wherein forming the charge storage layer comprises forming an ONO layer on the substrate.

23. (new) The method of claim 12, wherein forming the source electrode comprises:
forming a source electrode layer on the substrate; and
etching back the source electrode layer to form the source electrode.

24. (new) The method of claim 12, wherein forming the source electrode comprises:
forming a source electrode layer on the substrate; and

chemical mechanical polishing (CMP) the source electrode layer to form the source electrode.